SERIAL CLK IN/OUT: (SERIAL CLOCK IN/OUT)

This signal is used for timing the data sent on the serial bus. (See Figure 6-4).

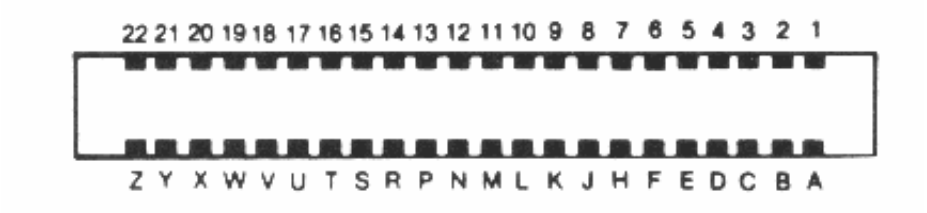
SERIAL DATA IN/OUT:

Data on the serial bus is transmitted one bit at a time on this line. (See Figure 6-4).

THE EXPANSION PORT

The expansion connector is a 44-pin (22/22) female edge connector on the back of the Commodore 64. With the Commodore 64 facing you, the expansion connector is on the far right of the back of the computer. To use the connector, a 44-pin (22/22) male edge connector is required.

This port is used for expansions of the Commodore 64 system which require access to the address bus or the data bus of the computer. Caution is necessary when using the expansion bus, because it's possible to damage the Commodore 64 by a malfunction of your equipment. The expansion bus is arranged as follows:



The signals available on the connector are as follows:

NAME	PIN	DESCRIPTION
GND	1	System ground
+5VDC	2	(Total USER PORT and CARTRIDGE devices can draw no more than 450 mA.)
+5VDC	3	
/IRQ	4	Interrupt Request line to 6502 (active low)
R/W	5	Read/Write (write active low)
DOT CLOCK	6	8.18 MHz video dot clock
/I/O1	7	I/O block 1 @ $ DE00-$DEFF (active low) unbuffered I/O
/GAME	8	active low ls ttl input
/EXROM	9	active low ls ttl input
/I/O2	10	I/O block 2 @ $DF00-$DFFF (active low) buff'ed ls ttl output
/ROML	11	8K decoded RAM/ROM block @ $8000 (active low) buffered ls ttl output
BA	12	Bus available signal from the VIC-II chip unbuffered 1 Is load max.
/DMA	13	Direct memory access request line (active low input) ls ttl input
D7	14	Data bus bit 7 - unbuffered, 1 ls ttl load max
D6	15	Data bus bit 6 - unbuffered, 1 ls ttl load max
D5	16	Data bus bit 5 - unbuffered, 1 ls ttl load max
D4	17	Data bus bit 4 - unbuffered, 1 ls ttl load max

D3	18	Data bus bit 3 - unbuffered, 1 ls ttl load max
D2	19	Data bus bit 2 - unbuffered, 1 ls ttl load max
D1	20	Data bus bit 1 - unbuffered, 1 ls ttl load max
D0	21	Data bus bit 0 - unbuffered, 1 ls ttl load max
GND	22	System ground
GND	A	
/ROMH	B	8K decoded RAM/ROM block @ $E000 buffered
/RESET	C	6502 RESET pin(active low) buff'ed ttl out/unbuff'ed in
/NMI	D	6502 Non Maskable Interrupt (active low) buff'ed ttl out, unbuff'ed in
02	E	Phase 2 system clock
A15	F	Address bus bit 15 - unbuffered, 1 ls ttl load max
A14	H	Address bus bit 14 - unbuffered, 1 ls ttl load max
A13	J	Address bus bit 13 - unbuffered, 1 ls ttl load max
A12	K	Address bus bit 12 - unbuffered, 1 ls ttl load max
A11	L	Address bus bit 11 - unbuffered, 1 ls ttl load max
A10	M	Address bus bit 10 - unbuffered, 1 ls ttl load max
A9	N	Address bus bit 9 - unbuffered, 1 ls ttl load max
A8	P	Address bus bit 8 - unbuffered, 1 ls ttl load max
A7	R	Address bus bit 7 - unbuffered, 1 ls ttl load max
A6	S	Address bus bit 6 - unbuffered, 1 ls ttl load max
A5	T	Address bus bit 5 - unbuffered, 1 ls ttl load max
A4	U	Address bus bit 4 - unbuffered, 1 ls ttl load max
A3	V	Address bus bit 3 - unbuffered, 1 ls ttl load max
A2	W	Address bus bit 2 - unbuffered, 1 ls ttl load max
A1	X	Address bus bit 1 - unbuffered, 1 ls ttl load max
A0	Y	Address bus bit 0 - unbuffered, 1 ls ttl load max
GND	Z	System ground

This page has been created by Sami Rautiainen.

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